REMARKS

In view of the above amendments and the following remarks, reconsideration of the rejections contained in the Office Action of May 15, 2007 is respectfully requested.

In the outstanding Office Action, the Examiner indicated that claims 14-16 and 24-35 are allowed, and the Applicants appreciate the Examiner's indication of this allowable subject matter. However, the Examiner also rejected previously allowed claims 18-23 in view of the prior art. Specifically, the Examiner rejected these claims as being unpatentable over the Enomoto reference (US Publication 2003/0032284). However, as indicated above, independent claim 18 has now been amended so as to slightly clarify the present invention recited therein. For the reasons discussed below, it is respectfully submitted that amended independent claim 18 and the claims that depend therefrom are clearly patentable over the prior art of record.

As explained on page 2, lines 10-12 of the original specification, a gate electrode which includes an SiN layer will prevent leakage. Unfortunately, exposure to high levels of heat during a subsequent heat treatment or subsequent operation often results in stress occurring between the layers of the gate electrode, thereby deteriorating the bond between the layers and possibly resulting in the pealing off of the SiN layer.

As now recited in amended independent claim 18, the gate electrode formed on the semiconductor substrate has *a tungsten silicide layer, a metallic polysilicon layer under the tungsten silicide layer, and an SiN layer on the tungsten silicide layer* (see Figure 1(c) and page 6, lines 2-15 of the original specification). Furthermore, a spacer consisting of an oxide film is formed on *a side wall of the gate electrode*. Therefore, a multi-layer gate electrode including an SiN layer is provided to reduce leakage, while the sidewalls of the multi-layer gate electrode are protected from abnormal oxidation and pealing, even if the gate electrode encounters subsequent high temperatures (see page 4, lines 12-16 of the original specification).

The Enomoto reference is directed to a method of fabricating a semiconductor integrated circuit, and the Examiner asserted that the Enomoto reference teaches a process of forming a gate electrode 7 including a tungsten silicide layer 13 on a semiconductor substrate 1. However, the Enomoto reference does not teach or even suggest forming a gate electrode on a semiconductor

substrate, in which the gate electrode has a tungsten silicide layer, a metallic polysilicon layer under the Tungsten silicide layer, and an SiN layer on the tungsten silicide layer, as now recited in amended independent claim 18. Because there is not even a suggestion of these features, there would be no apparent reason for one of ordinary skill in the art to modify the Enomoto reference so as to obtain the invention as recited in amended independent claim 18. Accordingly, it is respectfully submitted that amended independent claim 18 and dependent claims 19-23 are now clearly patentable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. However, if the Examiner should have any comments or suggestions to help speed the prosecution of this application, the Examiner is requested to contact the Applicant's undersigned representative.

Respectfully submitted,

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